Pre Amdt A
R. Webb
5-30-98

[2885/10]

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|---|
| Inventor(s) | : | Martin VORBACH et al. |
| Serial No. | : | 08/947,254 |
| Filed | : | October 8, 1997 |
| For | : | I/O AND MEMORY BUS SYSTEM FOR DFPs AND UNITS WITH TWO- OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES |
| Examiner | : | To Be Assigned |
| Art Unit | : | To Be Assigned |

Assistant Commissioner
for Patents
Washington D.C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

Date: 24 March 1998 Reg. No. 36,098

Signature: _____
Michelle M. Carniaux

**PRELIMINARY AMENDMENT**

SIR:

Kindly amend the above-identified application before examination, as set forth below.

**In the Specification:**

Please replace the original specification with the attached substitute specification.

**In the Abstract:**

Please delete the original abstract, and insert in its place the following: